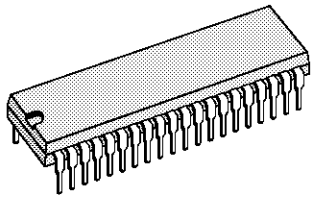
SGS-THOMSON MICROELECTRONICS

STV3200

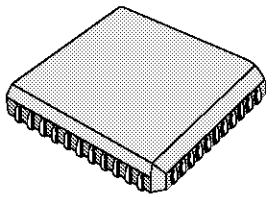
DISCRETE COSINE TRANSFORM (DCT)

- 0 TO 15.0 MHz OPERATING FREQUENCY EQUAL TO PIXEL RATE
- FORWARD OR INVERSE TRANSFORM
- 7 BLOCK SIZE POSSIBILITIES :
  16 x 16 8 x 8 4 x 4
  16 x 8 8 x 4
  8 x 16 4 x 8
- 9-BIT TWO'S COMPLEMENT PIXEL FORMAT CORRESPONDING TO 3 POSSIBLE MAGNITUDES DEPENDING ON THE PIXEL RANGE PIN (PR) STATE :
  - 8-BIT UNSIGNED MAGNITUDE
  - 8-BIT 2's COMPLEMENT MAGNITUDE
  - 9-BIT 2's COMPLEMENT MAGNITUDE
- 12-BIT TWO'S COMPLEMENT COEFFICIENT FORMAT
- FULLY TTL AND CMOS COMPATIBLE
- CMOS TECHNOLOGY
- SINGLE + 5 VOLTS POWER SUPPLY
- POWER DISSIPATION : 500 mW AT 15.0 MHz



DIP40
(Plastic Package)

ORDER CODE : STV3200P



PLCC44
(Plastic Chip Carrier)

ORDER CODE : STV3200FN

DESCRIPTION

The STV3200 is a dedicated circuit for the discrete cosine transform (DCT) computation. The two-dimensional forward DCT (FDCT) or inverse DCT (IDCT) is performed for various block sizes and a pixel rate up to 15.0 MHz. The circuit architecture is fully bidirectional with a 9-bit magnitude pixel data bus and a 12-bit magnitude coefficient data bus programmed as input or output depending on the selection of FDCT or IDCT.

	FDCT	IDCT	Data Format
Pixel Bus	Input	Output	9-bit 2's Complement
Coefficient Bus	Output	Input	12-bit 2's Complement

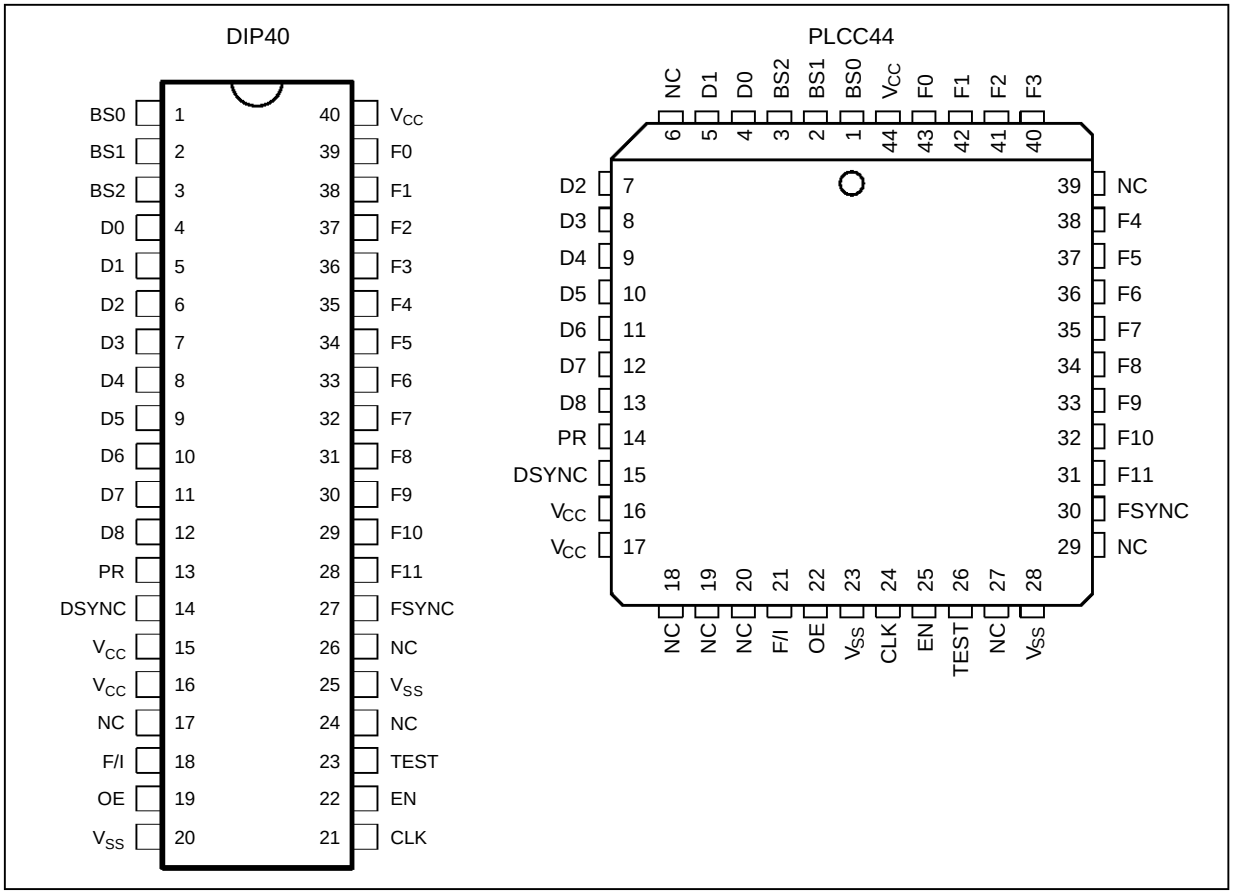
For the forward transform, the input pixels are coded in 9-bit 2's complement and the output coefficients are coded in 12-bit 2's complement. For the inverse transform, the data format is identical with the coefficients used as input and the pixels used as output.

ORDER CODES

Part Number	Temperature Range	Package
STV3200CP	0 to 70°C	DIP 40
STV3200CFN	0 to 70°C	PLCC44

3200-01.TBL

PIN CONNECTIONS



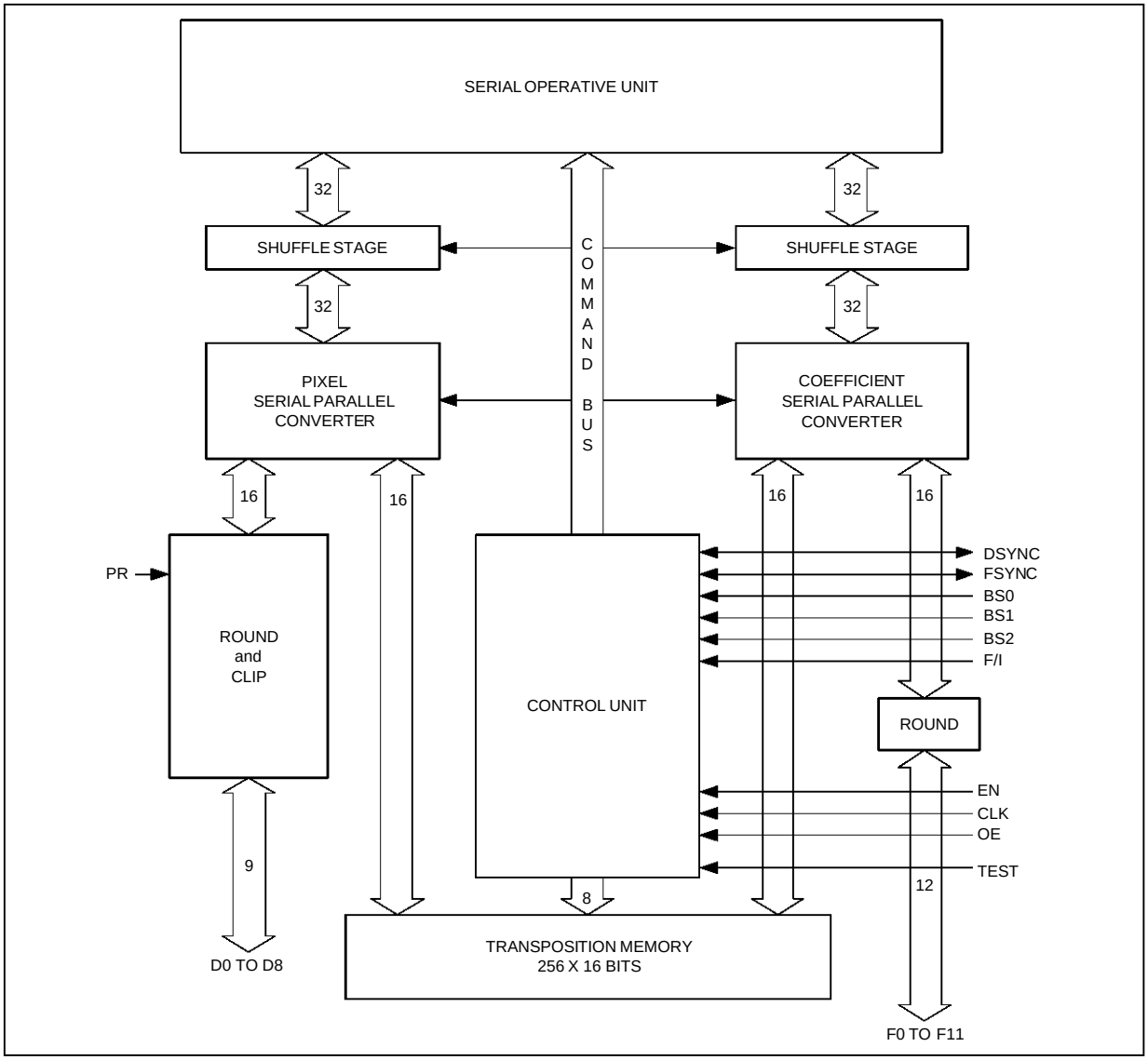
3200-01A.EPS / 3200-01B.EPS

PIN DESCRIPTION

DIP40	PLCC44	Symbol	Direction	Function
1 : 3	1 : 3	BS0 to BS2	IN	Block Size Selection
4 : 12	4 : 5 , 7 : 13	D0 to D8	IN / OUT	Pixel Data Bus
13	14	PR	IN	Pixel Range Selection
14	15	DSYNC	IN / OUT	Pixel Block Synchronization
18	21	F/I	IN	Forward or Inverse Transform Selection
19	22	OE	IN	Tristate Output Control
20 - 25	23 - 28	V_{SS}		Ground
21	24	CLK	IN	Clock Input
22	25	EN	IN	Clock Enable
23	26	TEST	IN	Test Mode
27	30	FSYNC	IN / OUT	Coefficient Block Synchronization
28 : 39	43 : 40 , 38 : 31	F0 to F11	IN / OUT	Coefficient Data Bus
40 - 15 - 16	16 - 17 - 44	V_{CC}		+ 5V ± 10%
17 - 24 - 26	6 - 18 - 19 - 20 27 - 29 - 39	NC		Not Connected

3200-02.TBL

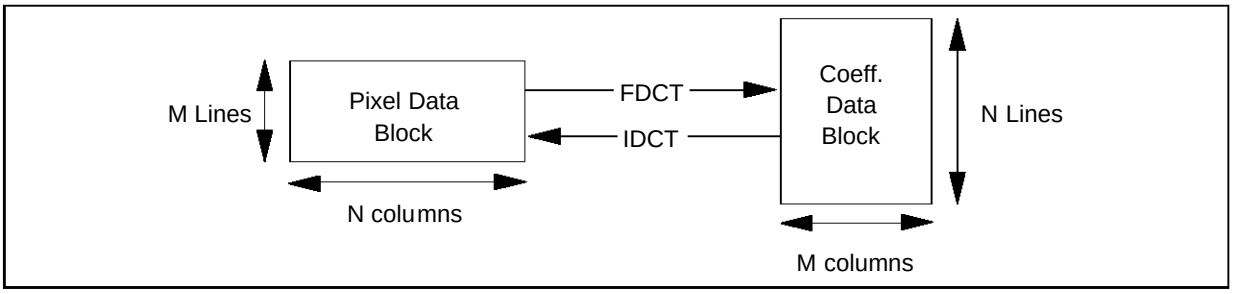
FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1 - EQUATIONS

Figure 1



The STV3200 performs a Two dimensional Discrete Cosine Transform according to the following equations, where the block size is defined by M lines and N columns of pixels :

FORWARD TRANSFORM EQUATION :

$$F(u,v) = \text{Round}\left[\frac{32}{N \cdot M} C^2(u)\, C^2(v) \sum_{i=0}^{M-1} \sum_{j=0}^{N-1} D(i,j) \cos\frac{(2 \cdot i + 1)\, u\, \pi}{2 \cdot M} \cos\frac{(2 \cdot j + 1)\, v\, \pi}{2 \cdot N}\right]$$

where C2(u) = 1/2 if u = 0
= 1 otherwise

INVERSE TRANSFORM EQUATION :

$$D(i,j) = \text{Round}\left[\frac{1}{8} \sum_{V=0}^{N-1} \sum_{u=0}^{M-1} F(u,v) \cos\frac{(2 \cdot i + 1)\, u\, \pi}{2 \cdot M} \cos\frac{(2 \cdot j + 1)\, v\, \pi}{2 \cdot N}\right]$$

2 - BLOCK FORMAT

M·N is the block size. This means that pixel blocks contain N columns of M pixels. The STV3200 performs a block transposition, and therefore the coefficient blocks contain M columns of N pixels.

The seven different possible block sizes are : 16 x 16, 8 x 16, 16 x 8, 8 x 8, 4 x 8, 8 x 4 and 4 x 4.

3 - BLOCK SCANNING

Many possible arrangements for pixel block scanning are possible. These different arrangements are :

A - the block is entered line by line from the top line to the bottom line. Each line is entered from the left pixel to the right pixel.
B - the block is entered line by line from the top line to the bottom line. Each line is entered from the right pixel to the left pixel.
C - the block is entered line by line from the bottom line to the top line. Each line is entered from the left pixel to the right pixel.
D - the block is entered line by line from the bottom line to the top line. Each line is entered from the right pixel to the left pixel.
E - the block is entered column by column from the left column to the right column. Each column is entered from the top pixel to the bottom pixel.
F - the block is entered column by column from the left column to the right column. Each column is entered from the bottom pixel to the top pixel.
G - the block is entered column by column from the right column to the left column. Each column is entered from the top pixel to the bottom pixel.
H - the block is entered column by column from the right column to the left column. Each column is entered from the bottom pixel to the top pixel.

4 - DATA FORMAT

The coefficient format is 12-bit 2's Complement, corresponding to the range – 2048 to 2047.

There are 3 possible ranges for pixel data :

8-Bit Unsigned Pixel Magnitude
(see Figure 2)
The pixel data range is 0 to 255. In this case D8 is always equal to 0 and the PR pin must be set to 1 for FDCT and IDCT. A clipping to the range 0 to 255 is performed before outputting the reconstructed pixels after an IDCT.

8-Bit Two's Complement Magnitude
(see Figure 3)
The input pixel data range is – 256 to 255 and a clipping to the range – 128 to 127 is performed internally just before the FDCT. In this case, the PR pin must be set to 0 for FDCT and IDCT.

9-Bit Two's Complement Magnitude
(see Figure 4)
The input pixel data range is – 256 to 255 and no clipping is performed. In this case, the PR pin must be set to 1 for FDCT and 0 for IDCT. Internal overflows may occur leading to aberrant errors on reconstructed values.

Figure 2

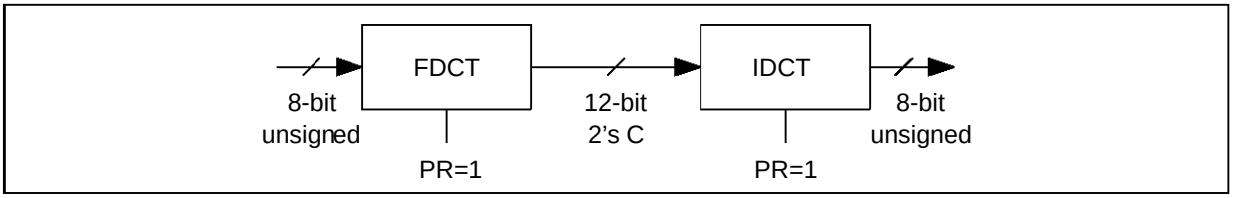


Figure 3

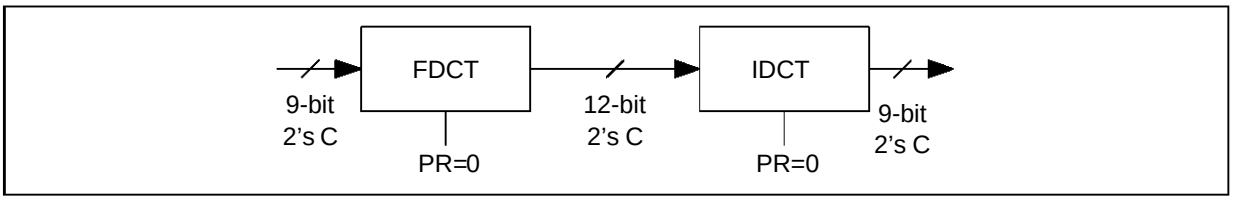
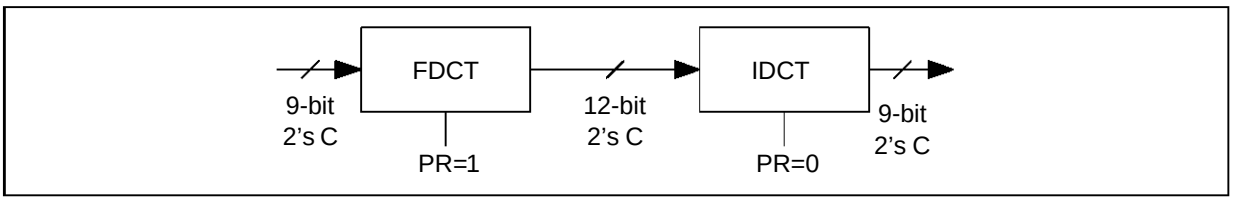


Figure 4



5 - BLOCK FLOW

Depending on the application, blocks may be entered in different ways.

Latent period : the latent period between input data and the corresponding output results in 130 + M·N cycles. This means that the first data item of a resulting block is provided 130 + M·N clock cycles after the first data item of the corresponding input block.

Synchronization signals : an input block synchronization signal must be provided. The input pin for this signal is DSYNC if FDCT is selected and FSYNC if IDCT is selected. This signal must be active with the first data item of each input block or group of blocks.

An output block synchronization signal is provided. The output pin for this signal is FSYNC if FDCT is selected and DSYNC if IDCT is selected. This signal is active with the first data item of each output block or group of blocks.

The output synchronization signal is equal to the input synchronization signal delayed from 130 + M·N clock cycles.

Continuous Block Flow

Input data is entered continuously with one new item data at each clock cycle and output data is provided continuously with one new result data item at each clock cycle.

The input synchronization pulse can be provided for each input block. In this case the output synchronization pulse is provided for each output block (Figure 5). Another way is to provide a synchronization pulse only for the first block. In this case, only one synchronization pulse is provided for the first output block (Figure 6).

Figure 5 : Continuous Block Flow-1

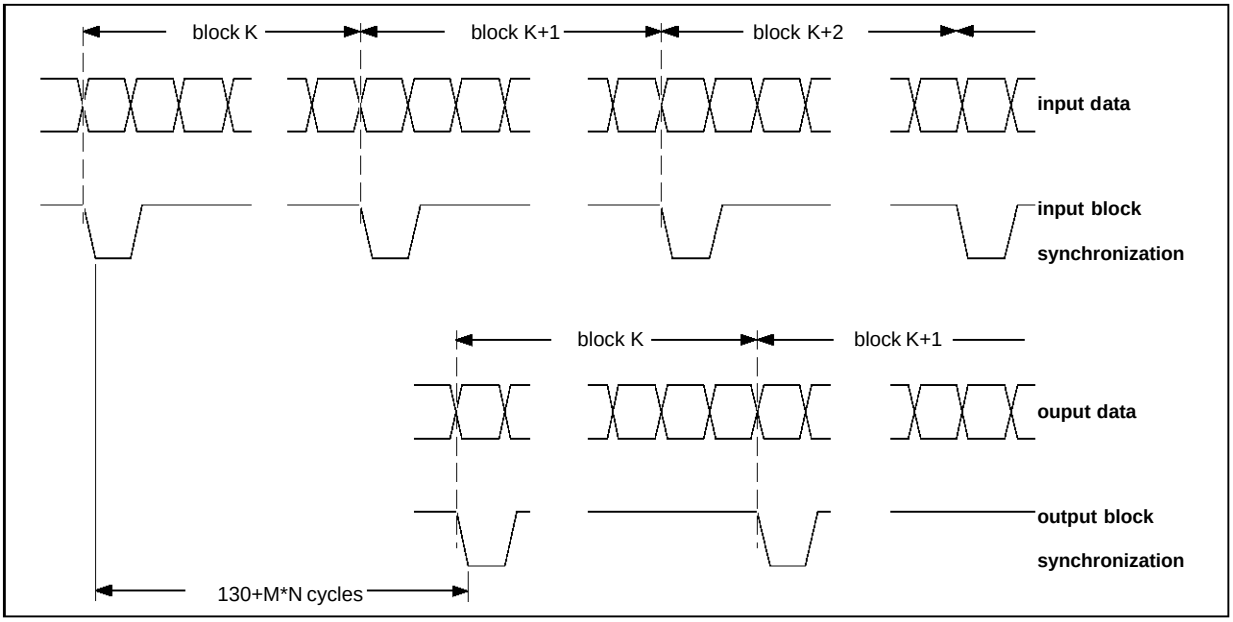
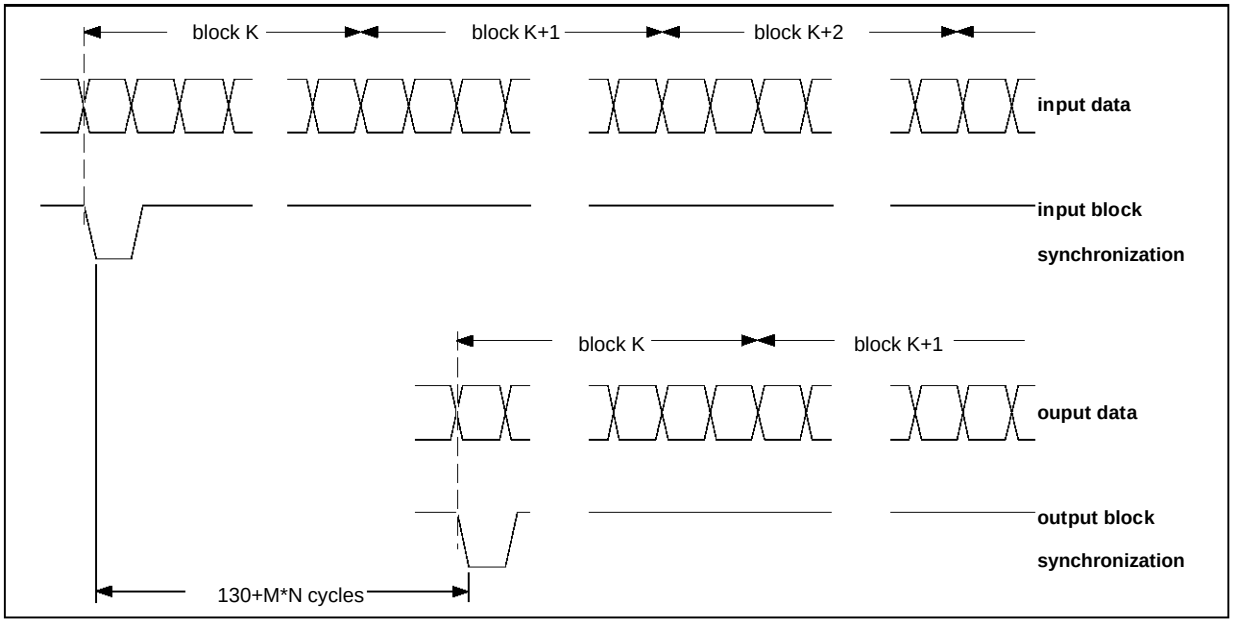


Figure 6 : Continuous Block Flow-2



Continuous Block Flow With Bypass of Irrelevant Data

It is possible to process a block flow including irrelevant data (corresponding to line suppresssion for example) as if it was a continuous block flow. One way is to stop the clock signal during the irrelevant data occurrence. Another way is to use the Clock Enable Signal (EN) to inhibit the chip internal clock during irrelevant data occurrence (Figure 7).

Burst Block Flow (see Figure 8)
Single blocks (or groups of blocks) may not be contiguous. In other words, delay cycles between two blocks (or groups of blocks) may exist. During these delay cycles, the clock is still running and the chip continues to perform computations. The constraint is that the internal pipe line must not be broken when a new block occurs. To take this constraint into account, the number of delay cycles (NC) must respect one of the following conditions :

1 - the number of delay cycles (NC) is greater than or equal to 130 + M·N. In this case the pipe line is empty (all the relevant data has been outputted) when a new input block processing starts.

2 - the number of delay cycles (NC) is a multiple of the number of cycles required to enter a block (M·N). In this case, the input data always remains synchronous with the internal pipe line.

Mixed FDCT/IDCT (see Figure 9)
In some low frequency applications, it could be useful to use only one chip to compute all the FDCT and IDCT required by the coding scheme. Blocks must be entered in a burst fashion with at least 130 + M·N delay cycles between the last item of the set of input pixels for FDCT and the first item of input coefficients for IDCT. The same delay must be respected between the last item of input coefficients for IDCT and the first pixel of input pixels for FDCT.

Figure 7 : Continuous Block Flow with Irrelevant Data

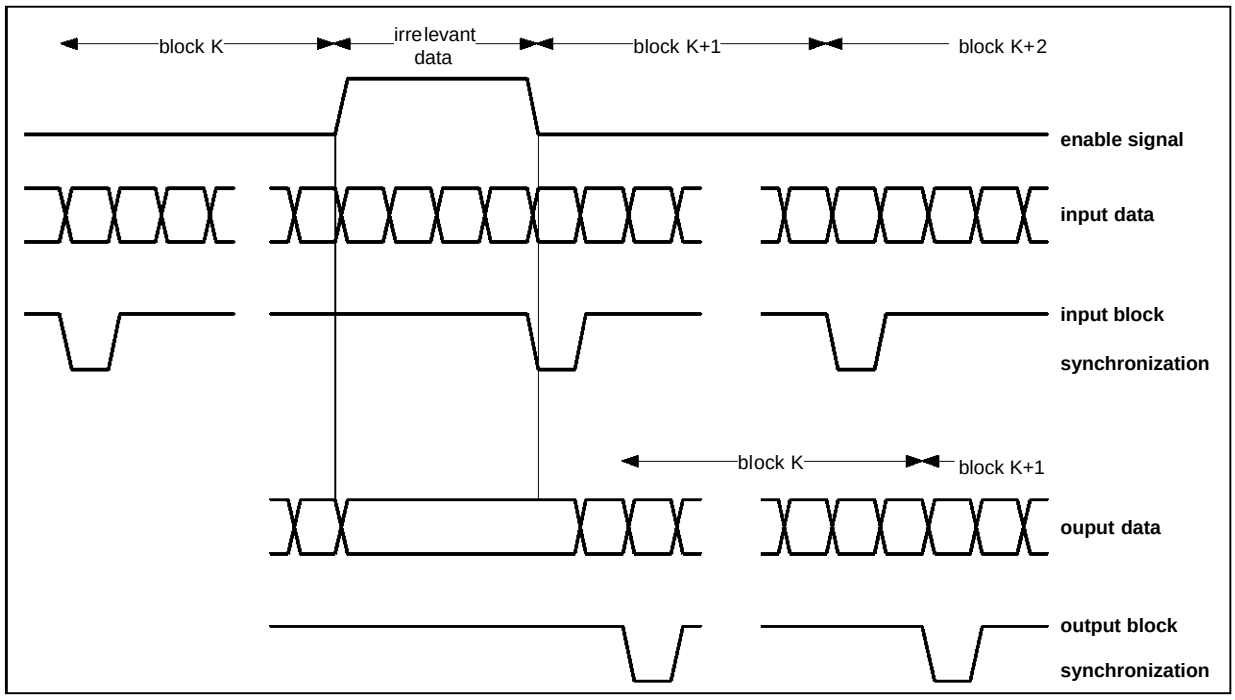


Figure 8 : Burst Block Flow

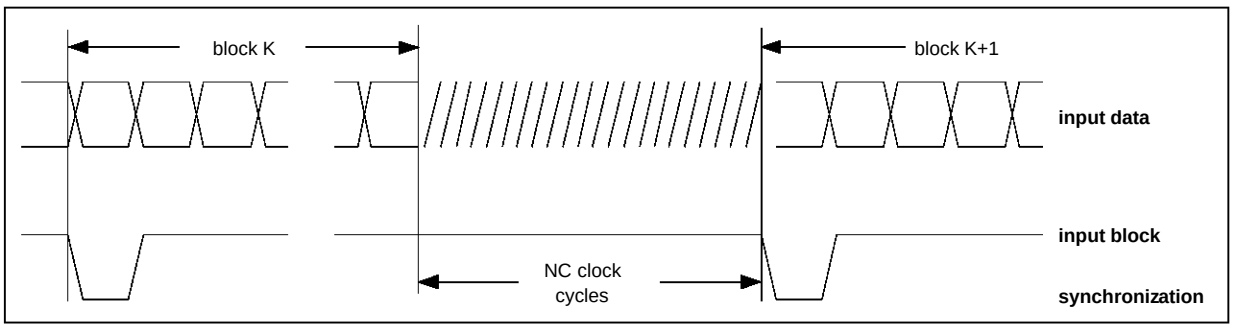
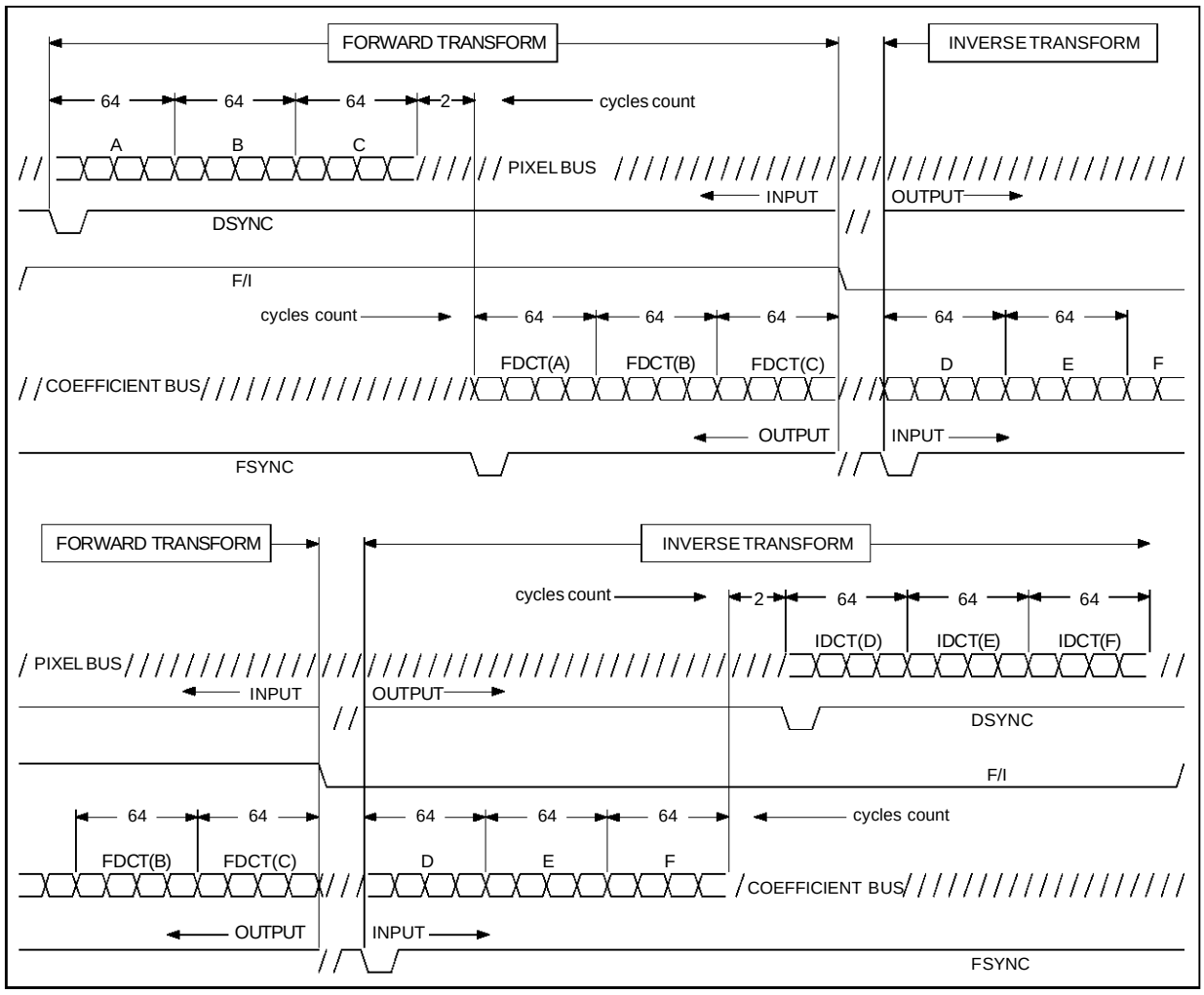


Figure 9 : Mixed 8x8 FDCT/IDCT Example Waveforms



6 - PINS DESCRIPTION

CLK : Clock signal

DATA PINS

D0 TO D8 : 9-bit bidirectional Pixel data bus pins. Direction is programmed by the F/I pin :

F/I State	D0 to D8 Direction
High	Input
Low	Output

Data is loaded (when input) on the falling edge of CLK or settled (when output) on the rising edge of CLK. D0 is the least significant bit and D8 the most significant one.

MSB								LSB	
D8	D7	D6	D5	D4	D3	D2	D1	D0	Pin
-256	128	64	32	16	8	4	2	1	Weight

DSYNC : Pixel data block synchronization signal. This pin is bidirectional with the direction programmed by the F/I pin (like D0 to D8). DSYNC is active (low level) with the first pixel data of a block (or group of blocks).

F0 TO F11 : 12-bit bidirectional Coefficient data bus pins. Direction is programmed by the F/I pin :

F/I State	F0 to F11 Direction
High	Input
Low	Output

Data is loaded (when input) on the falling edge of CLK or settled (when output) on the rising edge of CLK. F0 is the least significant bit and F11 the most significant one.

MSB											LSB	
F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0	Pin
-2048	1024	512	256	128	64	32	16	8	4	2	1	Weight

FSYNC : Coefficient data block synchronization signal. This pin is bidirectional with the direction programmed by the F/I pin like F0 to F11. FSYNC is active (low level) with the first coefficient data of block (or group of blocks).

CONTROL PINS

F/I : Forward or inverse selection. When F/I is high, forward DCT is performed. When F/I is low, inverse DCT is performed.

BS0 to BS2 : Block size selection. The block size is programmed through these three pins according to the following table :

BS0	BS1	BS2	Pixel Block Size	Coefficient Block Size
0	0	0	16 * 16	16 * 16
0	0	1	8 * 16	16 * 8
0	1	0	16 * 8	8 * 16
0	1	1	8 * 8	8 * 8
1	0	0	4 * 8	8 * 4
1	0	1	8 * 4	4 * 8
1	1	0	4 * 4	4 * 4
1	1	1	Reserved	

PR : Pixel range selection. This pin controls the clipping of the pixel data. If PR is high, output pixels of an IDCT are clipped to the range 0 to 255. If PR is low input pixels of an FDCT are clipped to the range – 128 to 127.

OE : Output enable. This signal is active low. When OE is high, all outputs (defined by the F/I pin state) are forced to the high impedance state.

EN : Enable. This signal is active low. When EN is high, internal states of the chip are frozen. When EN becomes low, execution restarts.

POWER SUPPLY AND GROUND PINS

V_{CC} : + 5 Volt power supply

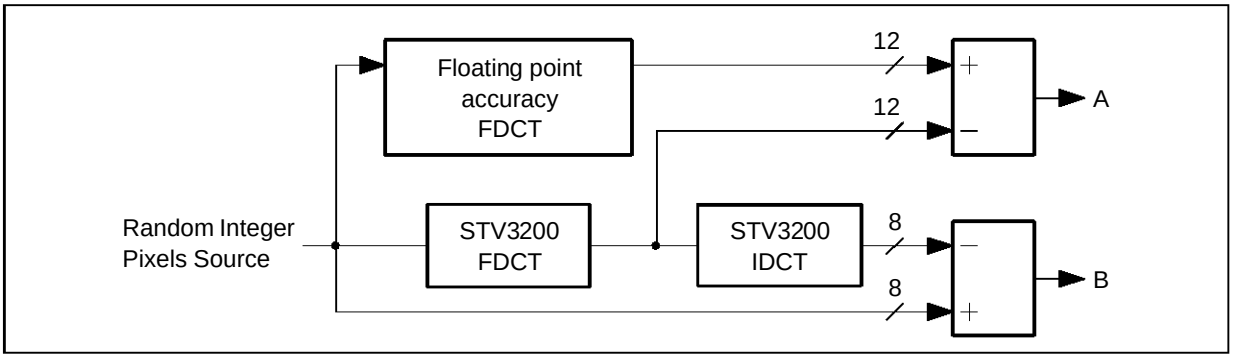
Vss : ground

OTHERS

TEST : test control. This pin is reserved and must be low in normal mode.

7 - ACCURACY CHARACTERISTICS

The accuracy characteristics have been measured according to the following scheme :



A : characteristics of FDCT for 8-bit magnitude random pixel data. Error between the FDCT computed with floating point accuracy and the FDCT computed by the STV3200 is measured.

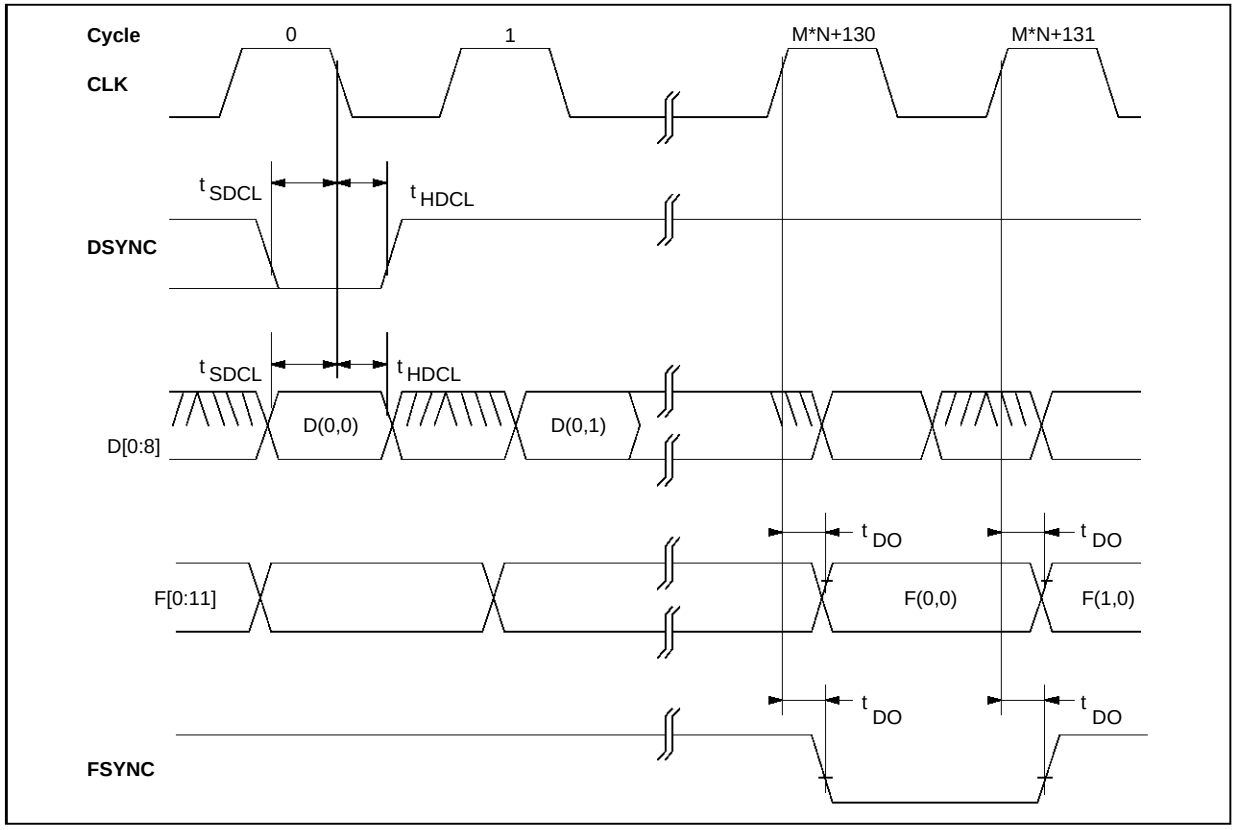
Block Size	16 * 16	8 * 16	16 * 8	8 * 8	4 * 8	8 * 4	4 * 4
Exact Value	86.8%	88.4%	86.9%	88.4%	89.4%	8.8%	91.0%
Error of ± 1LSB	13.0%	11.4%	13.0%	11.5%	10.5%	11.1%	8.9%
Error of ± 2LSB	0.23%	0.19%	0.14%	0.11%	0.11%	0.07%	0.11%

B : characteristics of FDCT followed by an IDCT for 8-bit magnitude random pixel data. Error between the source picture and the FDCT computed by the STV3200 followed by an IDCT computed by the STV3200 is measured.

Block Size	16 * 16	8 * 16	16 * 8	8 * 8	4 * 8	8 * 4	4 * 4
Exact Value	82.2%	93.9%	93.0%	99.0%	99.9%	99.9%	100%
Error of ± 1LSB	17.8%	6.1%	7.0%	1.0%	0.06%	0.08%	0%
Error of ± 2LSB	0.02%	0%	0%	0%	0%	0%	0%

TIMING WAVEFORMS

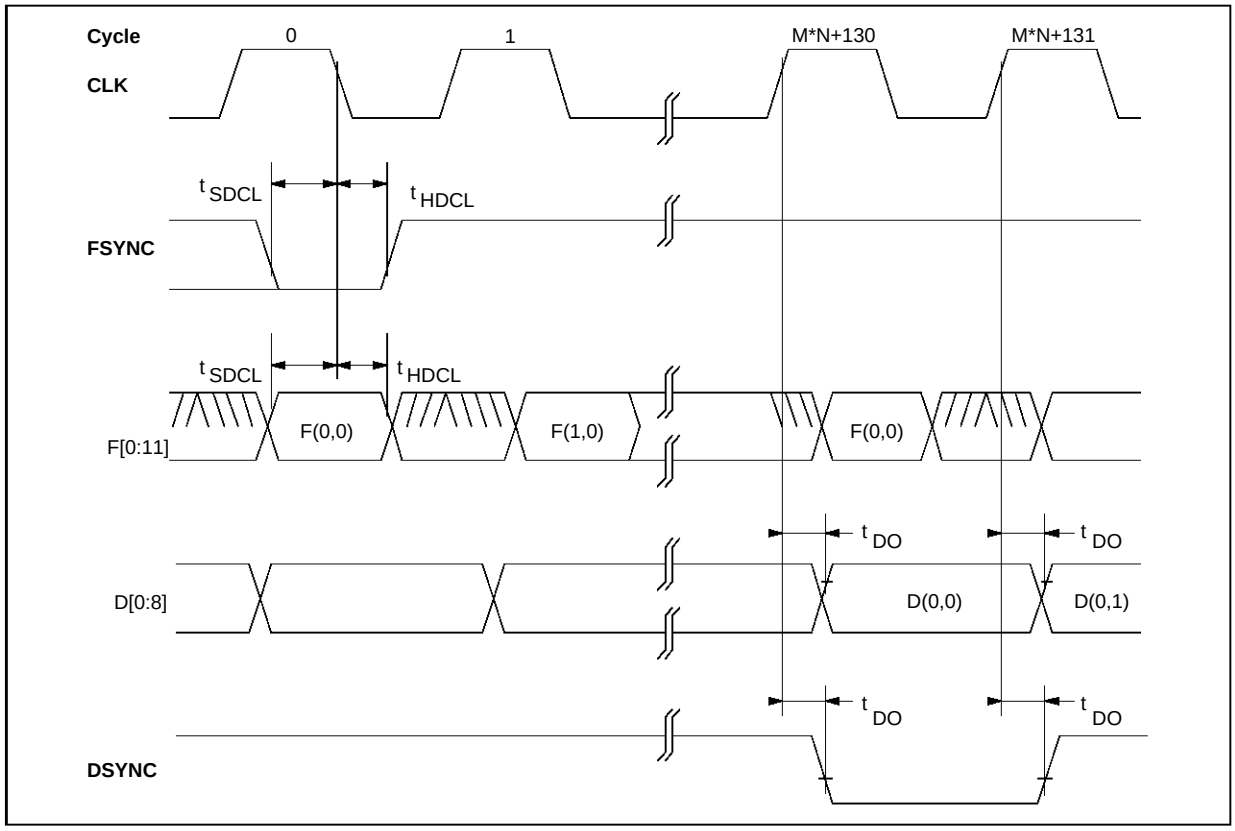
Sync Signals Timing Diagram for a Forward Transform on a M.N Block.



Note : FSYNC will be in an unknown state during the first 130 cycles after the power-up.

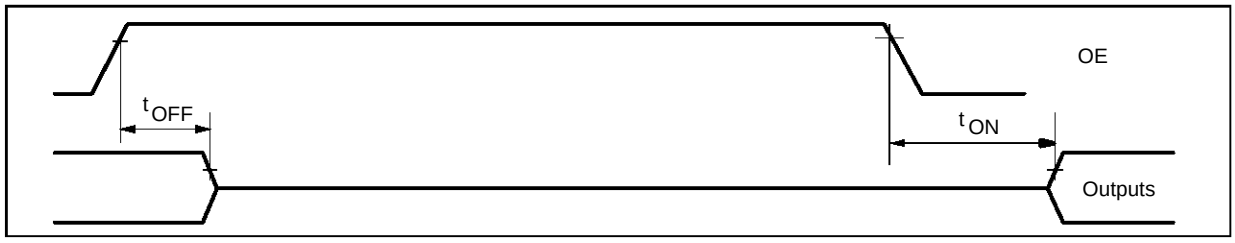
TIMING WAVEFORMS (continued)

Sync Signals Timing Diagram for a Inverse Transform on a M*N Block.

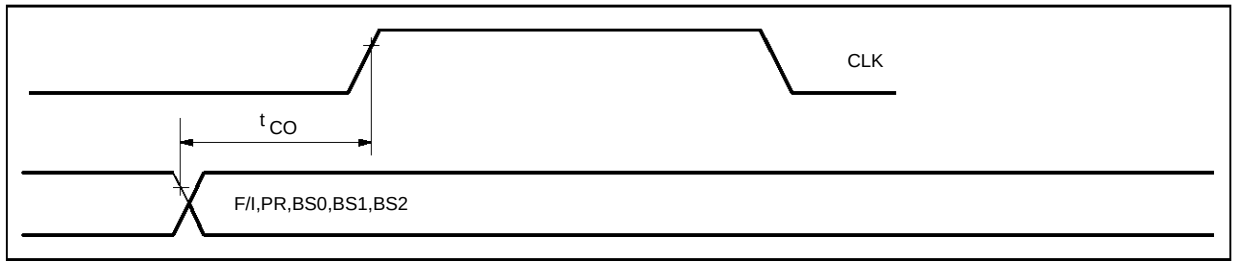


Note : DSYNC will be in an unknown state during the first 130 cycles after the power-up.

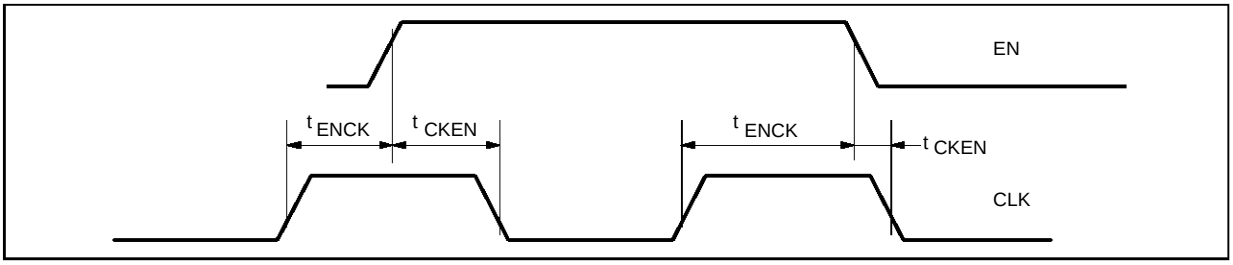
Outputs Enable Signal Timing Diagram



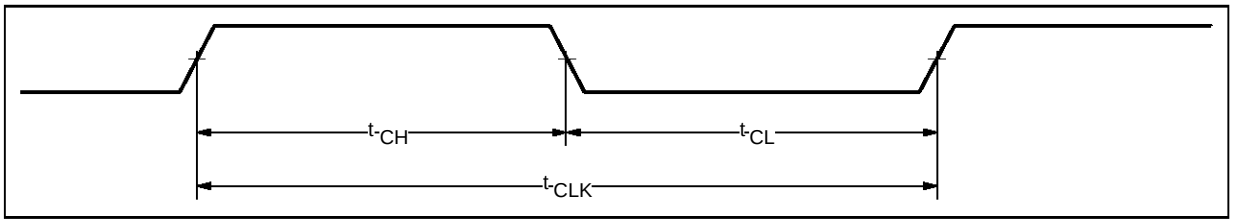
Control Signal Timing Diagram



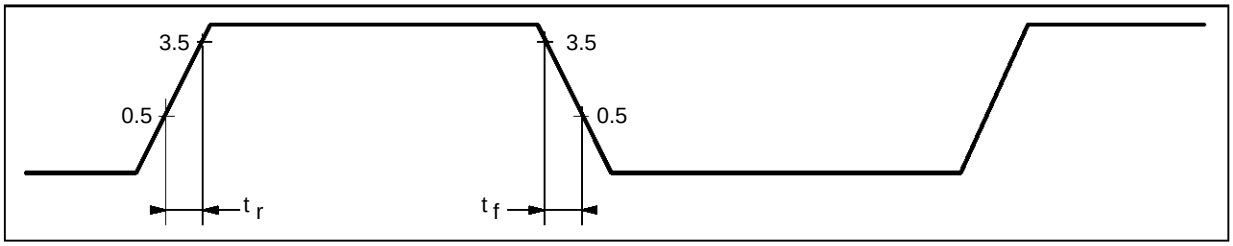
Enable Signal Timing Diagram



Clock Timing Diagram



Output Timing Diagram



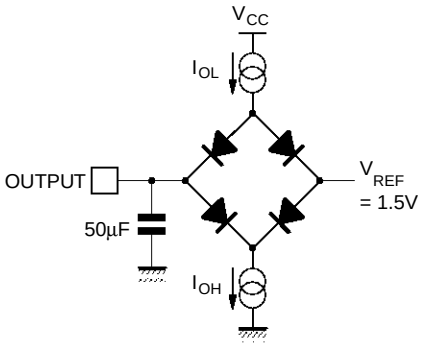
ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS
Supply voltage (V_{CC}) : 6 Volts
Operating Temperature Range : 0 to 70 °C
Voltage on Any Pin Relative to V_{SS} : – 0.5 to V_{CC} + 0.5 Volts

DC ELECTRICAL CHARACTERISTICS
Operating conditions : V_{SS} = 0 Volt, T_A = 0 to 70 °C, V_{CC} = 5V ± 10 % unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage		4.5		5.5	V
	Power Supply Ripple				0.5	V
I_{CC}	Supply Current f_{CLK} = 15MHz f_{CLK} = 0MHz	C_{LOAD} = 50pF on all output All inputs at V_{CC} or V_{SS}			 100 1	 mA mA
 V_{IL} V_{IH} 	Input Voltage Level (all inputs) Logic Low Logic High Hi-Z Input Leakage IN/OUT Buffers Input Buffers	V_{CC} = 5 ± 0.5 V_{IN} = V_{SS} to V_{CC}	 2 -5 -1		 0.8 +5 +1	 V V mA mA
 V_{OL} V_{OH}	Output Voltage Level (all outputs) Logic Low, ILOAD = +500µA Logic High, ILOAD = -500µA	V_{CC} = 4.5V	 2.7		 0.4 	 V V
C_{IN}	Input Capacitance	V_{offset} = 2.5V, f = 1MHz			10	pF

AC ELECTRICAL CHARACTERISTICS
Operating Conditions : V_{SS} = 0 Volt, T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 % unless otherwise noted
Outputs Load : capacitance = 50pF, current logic low = 500µA
Test Load on All Outputs :



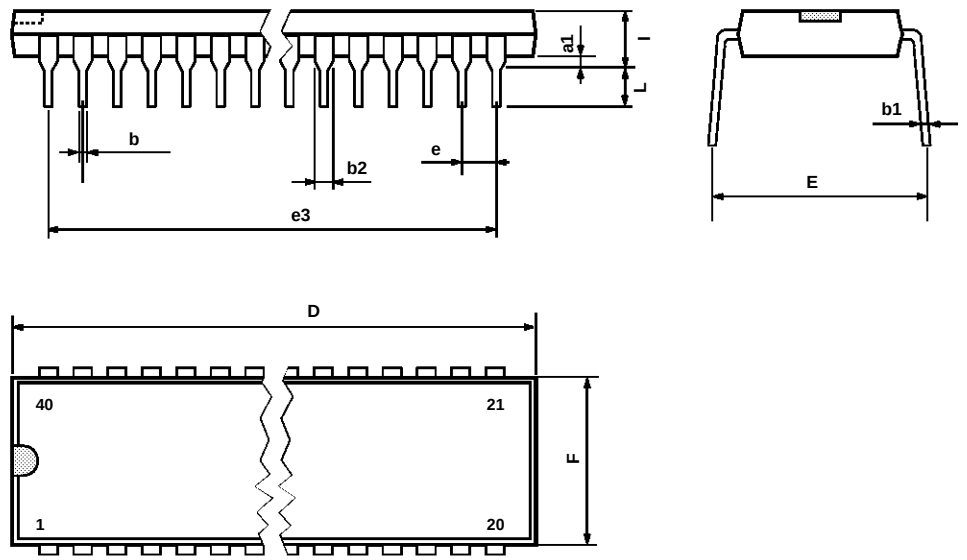
3200-20.EPS

Timings are measured between threshold voltage of 1.5 V unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_R	Rise Time from 0.5 to 3.5V			10	ns
t_F	Fall Time from 3.5 to 0.5V			10	ns
t_{CH}	Clock High Pulse Width	30			ns
t_{CL}	Clock Low Pulse Width	30			ns
t_{CLK}	Clock Cycle	66			ns
t_{SDCL}	Data Setup Time from CLK	5			ns
t_{HDCL}	Data Hold Time from CLK	20			ns
t_{DO}	Output Data Delay from CLK			33	ns
t_{CKEN}	Enable Hold from CLK	5			ns
t_{ENCK}	Enable Setup from CLK	5			ns
t_{OFF}	Delay from OE ↑ to Output going to High Impedance State			20	ns
t_{ON}	Delay from OE ↓ to Output going to High or Low State			20	ns
t_{CO}	Control Signal Setup from beginning of Input Stream	100			ns

PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



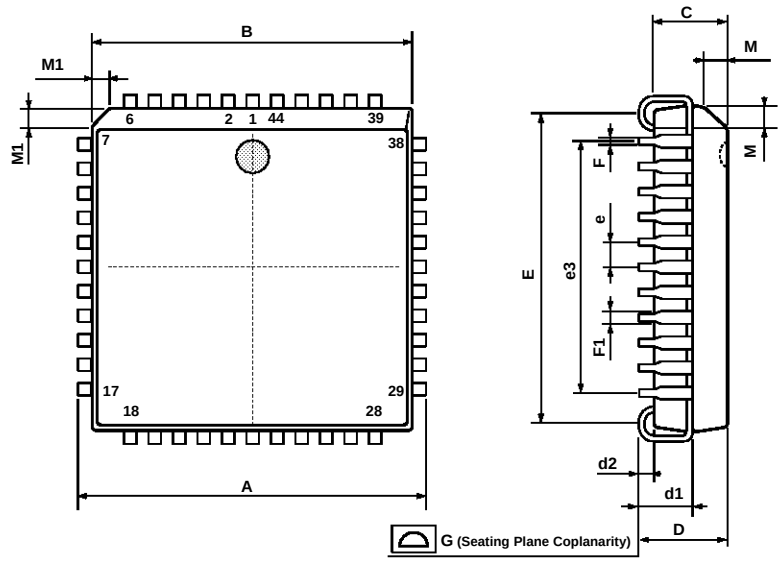
PM-DIP40.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP40.TBL

PACKAGE MECHANICAL DATA

44 PINS - PLASTIC CHIP CARRIER



PMPLCC44.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

PLCC44.TBL